IT 217 : Computer Organization

Credit Hours: *3*
Lecture Hours: 48

Course Objective:

This module aims to provide knowledge to understand the architecture of hardware components used in organization and design of digital computers and also design procedures of digital computers. Laboratory work is essential in this module.

Course Description:

Digital components used in the organization and design of digital computers, detailed steps that a designer must go through in order to design an elementary basic computer, the organization and architecture of CPU, I/O and Memory, Pipelining and Vector Processing, Concept of Multiprocessing.

Course Details

1. Data Representation — LH 3

1.1 Data Types
1.2 Complements
1.3 Fixed Point Representation
1.4 Floating Point Representation
1.5 End of Chapter 1 Assignment:
  1.5.1 Computer Program: Write program to visualize the representation of complement numbers, integers, floating point numbers and character data, overflow detection while adding binary data.

2. Register Transfer and Microoperations — LH 3

2.1 Register and Register Transfer Language
2.2 Bus and Memory Transfers
2.3 Arithmetic, Logic and Shift Micro-operations
2.4 Arithmetic Logic Shift Unit

3. Basic Computer Organization and Design — LH 7

3.1 Instruction Codes
3.2 Computer Registers
3.3 Computer Instructions
3.4 Timing and Control
3.5 Instruction Cycle
3.6 Input Output and Interrupt
3.7 End of Chapter 2 and 3 Assignment:
  3.7.1 Circuit Design: Design of Basic Computer

4. Programming the Basic Computer — LH 5

4.1 Introduction
4.2 Machine Language
4.3 Assembly Language
4.4 The Assembler
4.5 Program Loops
4.6 Programming Arithmetic and Logic Operations
4.7 Subroutines

4.8 Input Output Programming
4.9 End of Chapter 3 and 4 Assignment:
4.9.1 Computer Program: Develop assembler which can execute the program written for Basic Computer.

5. Microprogrammed Control LH 3

5.1 Control Memory
5.2 Address Sequencing
5.3 Microprogram Example
5.3.1 Computer Configuration
5.3.2 Microinstruction Format

6. Central Processing Unit LH 4

6.1 CPU Organizations
6.2 Instruction Formats
6.3 Addressing Modes
6.4 RISC and CISC Characteristics
6.5 End of Chapter 5 and 6 Assignment:
6.5.1 Computer Program: Write program to illustrate the use of different addressing modes.

7. Pipeline and Vector Processing LH 6

7.1 Parallel Processing, Flynn's Classification of Computers
7.2 Pipelining
7.3 Arithmetic Pipeline
7.4 Instruction Pipeline
7.5 Pipeline Hazards and Their Solution
7.6 Array and Vector Processing
7.7 End of Chapter 7 Assignment:
7.7.1 Case Study: Available array and vector processor; their application domain
7.7.2 Computer Program: write program which simulates instruction pipeline and arithmetic pipeline. Program generates space time diagram considering pipeline hazards.

8. Computer Arithmetic LH 4

8.1 Addition and Subtraction of Signed Magnitude Data
8.2 Addition and Subtraction of Signed 2's Complement Data
8.3 Multiplication of Signed Magnitude Data
8.4 Multiplication of Signed 2's Complement Data
8.5 End of Chapter 8 Assignment:
8.5.1 Computer Program: Implement all algorithms learned in this chapter.

9. Input and Output Organization LH 5

9.1 Peripheral Devices
9.2 I/O Interface
9.3 Asynchronous Data Transfer
9.4 Modes of Transfer
9.5 Priority Interrupt
9.6 Direct Memory Access
9.7 I/O Processor

9.8 End of chapter 9 Assignment:
9.8.1 Case Study: Device Independence I/O Software; USB (universal serial bus)

10. Memory Organization LH 4

10.1 Memory Hierarchy
10.2 Main Memory
10.3 Associative Memory
10.4 Cache Memory
10.5 Virtual Memory
10.6 Memory Management Hardware
10.7 End of Chapter 10 Assignment:
10.7.1 Computer Program: write program to visualize the advantage of using memory hierarchy.

11. Multiprocessor LH 4

11.1 Characteristics of Multiprocessor
11.2 Interconnection Structures
11.3 Inter Processor Arbitration
11.4 Inter Processor Communication and Synchronization
11.5 Cache Coherence
11.6 End of chapter 11 Assignment:
11.6.1 Case Study: ARM multicore processors and Intel multicore processors
11.6.2 Computer Program: Simulate cache coherence problem and simulate solution too.

Course Book

- M. Morris Mano, "***Computer System Architecture***", 3rd edition, Pearson Education Asia

References

- Andrew S. Tanenbaum, "***Structured Computer Organization***",4th edition, Prentice Hall Inc
- David A Patterson and John L. Hennesy, "***Computer Organization and design***"
- Sajjan G. Shiva, "***Computer Design And Architecture***", 3rd edition, Marcel Dekker Inc
- Daniel Page, "***A Practical Introduction to Computer Architecture***", *Springer*